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Mathematical modelling of tri-layer dielectric OTFT based on pentacene semiconductor for enhancing the electrical characteristics

Deepika Panghal[1]✉, Rekha Yadav[2]

[1,2] Deenbandhu Chhotu Ram University of Science and Technology, Sonepat, 131039, India

[1] deepikapanghal5@gmail.com✉, https://orcid.org/0000-0001-6769-0948
[2] rekhayadav.ece@dcrustm.org, https://orcid.org/0000-0001-9580-9766

Abstract
Organic thin film transistors (OTFTs) are significant for several reasons because their design processes are less complicated than those of conventional silicon technology which requires complex photolithographic patterning techniques and high-temperature and high-vacuum deposition processes. The more complex procedures used in traditional Si technology can be replaced by low-temperature deposition and solution processing. OTFTs based on the single-layer dielectric medium are poor in reducing the leakage current among the source and drain channel due to the incompatible resistance of dielectric medium. The paper presents a model of a tri-layer dielectric medium based on the organic semiconductor pentacene. In this tri-layer OTFT, three different dielectric mediums are used, such as SiO_2, POM-H (PolyOxyMethylene-Homopolymer) and PEI-EP (PolyEthyleneImine–Epoxy resin), for reducing the leakage current and enhancing the mobility among the source and drain channel. The parameter values, such as drain current I_{DS}, threshold voltage V_t and mobility for the designed tri-layer dielectric OTFT, are evaluated and compared with the single layer and bi-layer OTFT models. Thus, the attained mobility, drain current and threshold voltage for the proposed OTFT model are 0.0215 $cm^2/(V{\cdot}s)$, –4.44 mA for –10 V gate and –2.5 V drain voltage (V_{DS}) and threshold value 0.2445 V (V_t) for gate voltage –10 V (V_G). These attained parameter values are greater than the single- and bi-layer dielectric OTFT models. Thus, the mathematical modeling of the designed tri-layer dielectric OTFT model enhances the electrical characteristics of the other OTFT models.

Keywords
OTFT, SiO_2, PEI-EP, POM-H, mobility, threshold voltage

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Математическое моделирование трехслойного диэлектрика OTFT на основе пентаценового полупроводника для улучшения электрических характеристик

Дипика Пангал [1]✉, Рекха Ядав[2]

[1,2] Университет науки и технологий Динбандху Чхоту Рам, Сонипат, 131039, Индия

[1] deepikapanghal5@gmail.com✉, https://orcid.org/0000-0001-6769-0948
[2] rekhayadav.ece@dcrustm.org, https://orcid.org/0000-0001-9580-9766

Аннотация
Органические тонкопленочные полевые транзисторы (Organic thin film transistors, OTFTs) широко используются по нескольким причинам. Процессы их проектирования менее сложны, чем при традиционной кремниевой технологии, которая требует особые методы фотолитографического формирования рисунка и процессов высокотемпературного и высоковакуумного осаждений. Наиболее трудоемкие процедуры, используемые в

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традиционной кремниевой технологии, могут быть заменены низкотемпературным осаждением и обработкой на твердый раствор. OTFT на основе однослойной диэлектрической среды имеют большой ток утечки между истоком и стоком из-за несовместимости сопротивлений диэлектрической среды. В работе представлена модель трехслойной диэлектрической среды на основе органического полупроводника пентацена. В трехслойном OTFT использованы три диэлектрические среды: SiO_2, POM-H (полиоксиметилен-гомополимер) и PEI-EP (полиэтиленимин-эпоксидная смола) для снижения тока утечки и увеличения подвижности между истоком и стоком. Выполнена оценка и сравнение значений параметров: тока стока I_{DS}, порогового напряжения V_t и подвижности μ для разработанного трехслойного диэлектрического OTFT с одно- и двухслойными моделями. Полученные значения параметров для разработанной модели OTFT при напряжении затвора V_G = –10 В составили: I_{DS} = –4,44 мА; μ = 0,0215 см²/(В·с) (для напряжения стока V_{DS} = –2,5 В) и V_t =0,2445 В. Полученные значения параметров оказались больше, чем в одно- и двухслойных диэлектрических моделях OTFT. Таким образом, математическое моделирование разработанной трехслойной структуры продемонстрировало улучшение электрических характеристик по сравнению с другими типами OTFT.

Ключевые слова

OTFT, SiO_2, PEI-EP, POM-H, подвижность, пороговое напряжение

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Introduction

Organic thin film transistors (OTFTs) are currently developing an increase in attention due to the low-temperature technique and affordable manufacture. Consequently, their ability for a variety of applications is growing, including large-area flexible electronics and affordable electronic components [1]. Their useful applications include flexible screens, RF identification tags, sensors, electronic paper, etc. Furthermore, the natural flexibility of OTFT with all-polymer architectures enables the development of flexible integrated circuits [2]. Organic and polymer microelectronic device fabrication methods include thermal evaporation, printing, spin coating, and lithography [3]. A number of printing processes, such as Ink-Jet Printing (IJP), screen printing, micro contact printing, are quite interesting. The IJP approach has been receiving more attention among these printing technologies because of the polymer devices produced based on the benefits of straightforward fabrication processes, compatibility with many substrates, low temperature processing and affordability [4]. A Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) and OTFT have similar operating principles.

However, the channel formation is different and operates in a voltage-controlled current source by applying a voltage between the gate and the source (V_G) [5]. At this point, the charge carrier accumulation process begins at the semiconductor and insulator interface helps for the generation of current as well as the flow of current when a voltage between the drain and the source (V_{DS}) is applied [6]. OTFT is combined using the gate dielectric and an organic semiconductor layer with electrodes that consist of source, gate and drain [7]. The arrangement of the gate dielectric can be either upward or downward that determines the structure of the OTFT. Hence, the organic semiconductor layer source and drain contacts are referred to as Top Gate (TG) and Bottom Gate (BG) based on their location and contact structures [8]. Complex integrated circuits based on OTFTs need to be characterized and modeled in advance for efficient design.

Many mathematical models of the OTFTs have been created in recent years. They mostly utilize models of conventional Metal Oxide Semiconductor (MOS) transistors that have been slightly changed by the addition of suitable experimental factors [9]. The created model need to exhibit strong efficiency in circuit simulations and sufficient accuracy in device simulations. In reality, the design must consider the material specifications and the physical foundations of the device structure. However, innovation is still in its early stages and a variety of parameters including materials and structure that can change the established model by upgrading [10]. Therefore, it's crucial to take a hands-on approach to make the model update easier. Implicit equations are included in the model because of the physical treatment with surface potential variables. Model convergence in circuit simulations will rarely be affected by this technique. Hence, The OTFT model should be derived based on the explicit equations to prevent this divergence [11]. In this paper, the parameters of the OTFT, such as capacitor factor, mobility and threshold voltage, are mathematically modeled based on the different combinations of dielectric layer, such as SiO_2, PolyOxyMethylene-Homopolymer (POM-H) and PolyEthyleneImine–Epoxy resin (PEI-EP), to analyze the performance of the OTFT using $F_{16}CuPc$ semiconductor material. The derived parameters of the OTFT device for three different dielectric layers are used for finding the electrical characteristics. These electrical characteristics for each combinations of dielectric layer are derived and compared. As a result, the tri-layer dielectric OTFT will have better electrical properties than the existing OTFT. Major contributions of the designed model are:

- Mathematical modeling of tri-layer OTFT is derived for enhancing the electrical properties of the OTFT.
- Organic semiconductor pentacene, or $F_{16}CuPc$, is used to examine the effectiveness of the developed tri-layer dielectric OTFT.
- Insulating or dielectric medium including PEI-EP, POM-H and SiO_2 is used for enhancing the electrical conductivity between the source and drain.

— Parameters of the tri-layer OTFT, such as capacitor factor, mobility and threshold voltage, are mathematically determined.

Literature Review

Numerous techniques are introduced for enhancing the electrical conductivity between the source and drain channels which have been developed by using single-, bi- and tri-layer dielectric medium. The majority of current methods are studied and some of them are reviewed below Borthakur and Sarma [12] had designed OTFT based on top contact pentacene with bi-layer source drain electrode. The dielectric medium used in this model are N, N^′-Bis (3-methyl phenyl) — N, N^′-diphenyl benzidine with TPD/Au bi-layer source-drain (S-D) electrodes. This bi-layer electrode shows better performance than the single-layer S-D electrode OTFT devices. The field-effect mobility, "on–off" ratio, threshold voltage and the subthreshold voltage, are attained from the designed model with TPD/Au bi-layer source-drain electrode.

Cortes-Ordonez et al., [11] had developed an analytical and compact model of gate capacitance in OTFT. This modeling aims to validate compact capacitance of OTFTs at the accumulation from the depletion region by considering the frequency response. This OTFT is designed based on the Unified Model parameter Extraction Method (UMEM) to calculate the parameter values of the designed model. The effect associated with the density of localized states is included in the gate capacitance. Furthermore, experimental derivation of the gate capacitance and the presentation of this model forecast with a high accuracy.

Li et al., [13] had performed a mobility model based on temperature and contact resistance in organic thin-film transistors. A mobility model for OTFT is developed by taking into account contact and temperature resistance based on the device physics. The mobility model with hopping mechanism can explain that temperature and gate bias are dependent on the surface potential. It is also taken into account to determine the proper mobility when calculating the contact resistance. A DC compact model is designed for resisting the interface and temperature in the model at the range of –190 °C to 22 °C. The several comparisons among developed model and experimental data or numerical iteration provide strong evidence for the mobility and current models validity.

Cortes-Ordonez et al., [14] had performed extraction of parameter from I–V and C–V characteristics by modeling OTFTs with the temperature range of –123 °C to 77 °C. Analyses of the obtained parameters based on temperature dependency are performed. At various temperatures, an OTFT-adapted unified model and parameter extraction techniques are employed for finding the performance of the model. The experimental I-V characteristics in the linear and saturation regimes as well as the C-V characteristics at various frequencies are compared in order to validate this model.

Leise et al., [15] had developed an approach for the calculation of charges and capacitances in staggered OTFTs. The charges are produced in an analytical and concise manner using an existing DC model. To distribute charges among the drain and source sides of the channel, a linear charge partitioning system is used. The only factors that affect the final equation are the drain and source end charge densities of the channels with geometrical features. The capacitances are compared with the results of the Centaurus Technology Computer-Aided Design (TCAD) simulation and measurement data using the compact model which is implemented in Verilog A. This model has the advantage of having a singular formulation that accounts for all operational regimes.

Numerous dielectric polymers with single-, bi-, and tri-layers are used from the above-reviewed method to improve electrical performance. In existing techniques, the mathematical modeling of single-layer dielectric medium is used for OTFT to conduct the electric current from the source to drain electrode. In those OTFT, the mobility of the charge carriers of the OTFT is poor. Therefore, the tri-layer OTFT is mathematically created to improve the electrical performance of the OTFT and the mobility of charge carriers.

Proposed Methodology

In OTFT, the flow of current among the source and drain channel is produced by an inorganic dielectric such as silicone dioxide which is employed as a dielectric polymer. Using the inorganic dielectric layers, there are advantages as well as disadvantages in the OTFT. The advantages of the inorganic dielectric are addressing the scaling issues and reducing the leakage current in the short channel OTFTs, and the disadvantages are reduction in mobility with an increase in dielectric constant and high-surface energy that reduces the mobility further. Hence, the addition of organic dielectric layers to the inorganic dielectric will enhance the mobility and reduce the leakage current in the short channels. In this mathematical model, the tri-layer dielectric medium enhances electrical conductivity of the source and drain channel. The interior structure of the tri-layer OTFT is illustrated in Fig. 1.

The variables in the tri-layer OTFT are Thickness of the semiconductor (T_{OX}), Thickness of tri-layer dielectric medium (T_{OSC}), Source capacitance of oxide material ($C_{OV,S}$), Capacitive resistance for source ($R_{C,S}$), Gate Resistance (R_G), Gate to Source capacitance (C_{GS}), Gate to Drain capacitance (C_{GD}), Source to Drain Resistance (R_{SD}), Drain capacitance of oxide material *n* ($C_{OV,D}$) and

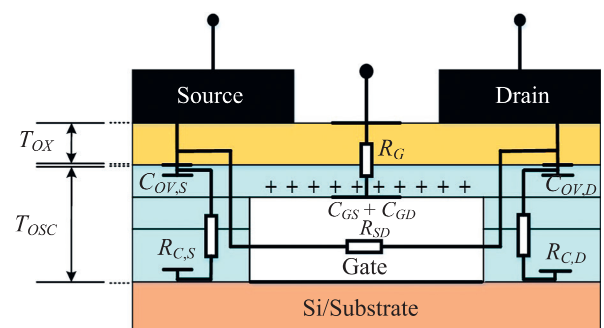

Fig. 1. Interior structure of the tri-layer OTFT (see below for notation definitions)

Capacitive resistance for Drain ($R_{C,D}$). In this model, the *n*-type heavily doped silicon wafer is used as a substrate. The gate dielectric, such as SiO_2, POM-H and PEI-EP, are used for controlling the flow of current at the source to drain channel. For evaluating the electric characteristics of the OTFT, an organic semiconductor such as $F_{16}CuPc$ and pentacene is used. Finally, the copper is used as the source and drain metal electrode. The parameters extracted from the mathematical modeling are Device threshold voltage (V_t), capacitive insulation (C_{ins1}, C_{ins2} and C_{ins3}) and Mobility (μ) for three dielectric medium are evaluated.

Mathematical modeling of OTFT for extracting the parameters

In this model, the work done is based on deriving the mathematical equations for single-, bi- and tri-layer dielectric medium based OTFT model to extract the electrical parameters of the OTFT. Bottom gate-top contact is the fundamental architecture of a transistor where the length is situated among the drain and source contacts. OTFT is simply a drift mechanism like the existing Complementary Metal Oxide Semiconductor technology where the linear and subthreshold regimes are controlled by using a single equation. The derived equation for the OTFT is based on the Variable Range Hopping (VRH) model. For unipolar charge carrier (electrons) the channel conductivity from equation is defined as

$$\sigma = e\mu n(y), \tag{1}$$

where $n(y)$ is the electron concentration in the channel, μ is the electron mobility defined as the charge velocity divided by the electric field. In the following equation, the mobility of electron is determined as

$$\mu = V/E.$$

Two powerful experiments are used to define the material charge mobility. The first is Time of Flight (TOF) where mobile charges are generated by photonic excitation. The charges are accelerated by external electric field (E). The mobility can be measured by the time (Δt), it takes the charges to move through a path of distance (L). Mobility of electrons at first TOF is determined using the following equation

$$\mu_{\text{TOF}} = \frac{L}{\Delta t E}.$$

Current density across the channel according to Ohm law is determined using the equation

$$J_x = \sigma E_x. \tag{2}$$

Substituting the equation (1) in (2) and integrating will give us the total channel current

$$I_x = \int_y \int_z J_x dy dz = \mu E_x \int_y en(y)dy \int_z dz. \tag{3}$$

The channel charge per unit area is defined in equation

$$Q_{\text{ch}} = -\int_y en(y)dy. \tag{4}$$

Substituting equation (3) in (4), the following equation and determines the total channel current.

$$I_x = -\mu E_x Q_{\text{ch}} \int_z dz$$
$$I_x = -\mu E_x Q_{\text{ch}} W, \tag{5}$$

where W is the channel width accepted by integration over z axis and $E_x = \frac{dV_x}{dx}$. The channel charge Q_{ch} per unit area is assumed to be constant across, and it is accumulated across the channel after flat band has achieved, which is determined at equation.

$$Q_{\text{ch}} = -C_{\text{ins}}(V_G - V_x - \Phi_{\text{ms}} - V_{\text{ins}}(\text{FB})), \tag{6}$$

where V_G is the gate to source potential, V_x is the potential in the channel at a point x and the C_{ins} is insulator capacitor per unit area. The insulator capacitor per unit is determined using the following equation

$$C_{\text{ins}} = \frac{\varepsilon_0 \varepsilon_{\text{ins}}}{t_{\text{ins}}},$$

where ε_0 and ε_{ins} are the permittivity of free space and relative insulator permittivity and t_{ins} is the insulator layer thickness. Fig. 2 shows the metal, insulator and semiconductor energy levels before physical contact.

Electron affinity of insulator (ex_i), Electron affinity of semiconductor (ex_s), Insulator gap energy (Eg_i), semiconductor gap energy (Eg_s), Fermi level for semiconductor (E_{Fs}), Fermi level for insulator (E_{Fi}), Potential difference between the intrinsic Fermi level and the doped Fermi level ($e\Phi_F$), Metal work function ($e\Phi_m$), Fermi level for metal (E_{Fm}). When metal, insulator and semiconductor materials are jointed together to form MIS capacitor, an equilibrium state occurs by Fermi level alignment between the metal work function and the semiconductor Fermi level (a short between the semiconductor bulk and the metal contact may be needed to promote this equilibrium). This equilibrium and the

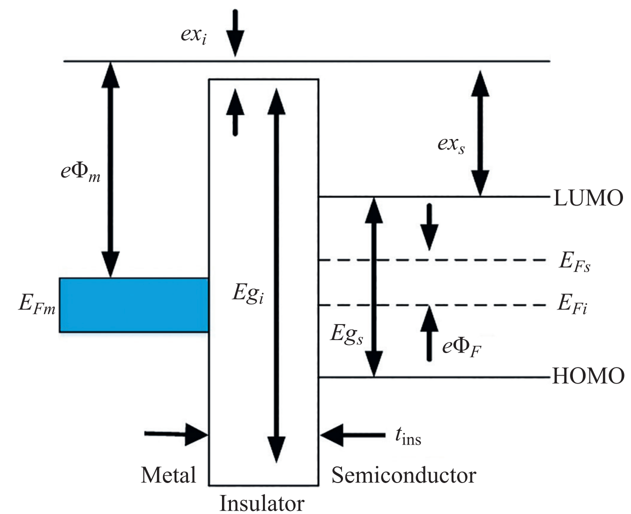

Fig. 2. Metal, insulator and semiconductor energy levels before physical contact

associated charging cause the HOMO and LUMO levels to bend near the interface between the semiconductor and the insulator. In addition, it causes a shift in the vacuum levels of the metal and the semiconductor. The existence of nonzero potential between the gate material and the semiconductor cause net charge to appear on both sides of the insulator. The metal-semiconductor work function difference Φ_{ms} is derived from equation

$$\Phi_{ms} = \Phi_m - (\chi_s + \frac{E_{gs}}{2q} - \Phi_F),$$

where Φ_m is the metal work function, χ_s is the semiconductor electron affinity, E_{gs} is the semiconductor gap energy, q is charge, and Φ_F is the potential difference between the intrinsic Fermi level and the doped Fermi level. In the case of non-degenerate semiconductors, it is defined by using the following equation:

$$\Phi_F = V_t \ln\frac{N_d}{n_i},$$

where V_t is the thermal voltage, N_d is the donor doping concentration, and n_i is the intrinsic carrier concentration. The contact potential effect (the different energy levels of the metal and semiconductor) is not the only one that causes net concentration of charges. A "parasitic" charge may exist in the insulator and influence the charge concentration in the MIS device.

If the "trapped" charge is defined as Q_{ss} and if we assume it is concentrated close to the insulator semiconductor interface (as appear in Fig. 3), then the induced potential drop across the insulator is defined by using the equation.

$$V_{ins} = \frac{Q_{ss}}{C_{ins}}.$$

In this equation, the MIS capacitor is in equilibrium without external potential that can sum the energy levels using the equation

$$-\Phi_{ms} = \Phi_{s0} - V_{ins0}. \quad (7)$$

If a gate voltage V_G is applied, then the potential drop across the insulator and the surface potential changes as per the following equation

$$V_G = \Delta V_{ins0} + \Delta\varphi_{s0} = (V_{ins} - V_{ins0}) + (\Phi_s - \Phi_{s0}). \quad (8)$$

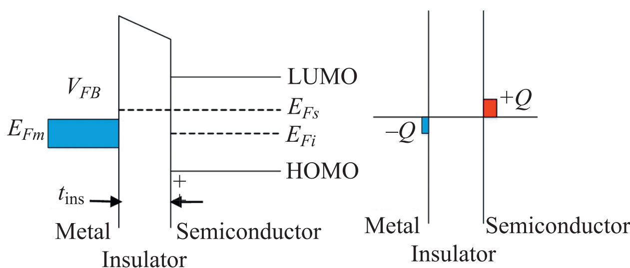

Fig. 3. Flat band conditions after applying external potential V_{FB}

By inserting equation (7) into (8), the gate voltage V_G will be converted to the following equation

$$V_G = V_{ins} + \Phi_s + \Phi_{ms}.$$

Flat band conditions exist when no charge is present in the semiconductor and the semiconductor energy bands are flat. In this condition, the surface potential equals to zero and the charge density on the gate metal should cancel the parasitic charge existing in the insulator as defined by the following equation

$$Q_{ss} + Q_m = 0.$$

Therefore, in flat band condition the gate potential is derived as equation

$$V_G(\mathrm{FB}) = V_{ins} + \Phi_{ms} = \frac{Q_{ss}}{C_{ins}} + \Phi_{ms}.$$

Hence, the flat band condition results in the threshold voltage in the form of the following equation

$$V_t = \frac{Q_{ss}}{C_{ins}} + \Phi_{ms} = \Phi_{ms} + V_{ins(FB)}. \quad (9)$$

Substituting the equation (9) in (6), we get the charge per unit as the following equation

$$Q_{ch} = -C_{ins}(V_G - V_x - V_t). \quad (10)$$

Substituting the equation (10) in (5) with $E_x = \frac{dV_x}{dx}$, we apply electric field among the drain and source contact. Then, the following equation defines the total channel current:

$$I_x = \mu\frac{dV_x}{dx}C_{ins}(V_G - V_x - V_t)W. \quad (11)$$

Integrating (11) over the channel length L and the drain source potential V_{DS}, the following set of equations is derived:

$$\int_0^L I_x = \int_{V_S}^{V_D} \mu\frac{dV_x}{dx}C_{ins}(V_G - V_x - V_t)W,$$

$$\int_0^L I_x dx = \int_{V_S}^{V_D} \mu W C_{ins}(V_G - V_x - V_t)dV_x,$$

$$I_x\int_0^L dx = \mu W C_{ins}\int_{V_S}^{V_D}(V_G - V_x - V_t)dV_x,$$

$$I_x = \mu\frac{W}{L}C_{ins}\int_{V_S}^{V_D}(V_G - V_x - V_t)dV_x.$$

Here, $V_{DS} = V_D - V_S$ and $I_x = I_{DS}$, and then

$$I_{DS,lin} = \mu\frac{W}{L}C_{ins}[V_G - V_t]V_{DS} - \frac{V_{DS}^2}{2}. \quad (12)$$

Equation (12) can be used as long as $|V_{DS}| < |V_G - V_t|$. This region is called the linear region. However, when drain-source voltage increases above this limit, section of

the channel (near the drain electrode) will move to depletion state cancelling charge accumulation at this zone. By increasing the drain-source voltage, the channel depletion zone enlarges. This bottleneck section limits the channel current by increasing the channel resistance associated with increasing the channel depletion that is affected by the drain-source voltage. In turn, this dependence causes the channel current to get into saturation region. For this case, integration of the boundaries is used, and the result looks like equation:

$$\int_0^{L_{\text{eff}}} I_{DS}(y)dy = \int_0^{V_G - V_t} W\mu C_{\text{ins}}(V_G - V_y - V_t)dv(y),$$

where L_{eff} is the effective channel length and $V_G - V_t$ is the voltage boundaries inside L_{eff}. For long channel transistor ($L >> d$ in lateral transistors) the depletion section is small compared to channel length ($L - L_{\text{eff}} << L$). So L_{eff} can be written as L. Integration of the equation results in

$$I_{DS}L = \mu W C_{\text{ins}}\left[[V_G - V_t]V - \frac{V^2}{2}\right]_0^{V_G - V_t} =$$

$$= \mu\frac{W}{L}C_{\text{ins}}\left[[V_G - V_t][V_G - V_t] - \frac{(V_G - V_t)^2}{2}\right] \quad (13)$$

$$I_{DS,sat} = \mu\frac{W}{2L}C_{\text{ins}}[V_G - V_t]^2.$$

Equation (13) can be used as long as $|V_{DS}| > |V_G - V_t|$. This region is defined as the saturation region. $\mu = \left(\frac{L}{W}\right)((St)V_G)$. Here, L and W are the length and width of the channel, St and V_G are the thickness of the semiconductor and gate voltage, respectively. In this model, three different layers of insulator are used, such as SiO_2, POM-H and PEI-EP, for enhancing the conductivity of current from source to drain channel by varying the gate and rain voltage. The following two equations are an illustration of the linear drain current for tri-layer OTFT.

$$I_{DS,lin} = \mu\frac{W}{L}\left[\frac{\varepsilon_0\varepsilon_{\text{SiO}_2}}{t_{\text{SiO}_2}} + \frac{\varepsilon_0\varepsilon_{\text{POM-H}}}{t_{\text{POM-H}}} + \frac{\varepsilon_0\varepsilon_{\text{PEI-EP}}}{t_{\text{PEI-EP}}}\right]\times$$

$$\times[V_G - V_t]V_{DS} - \frac{V_{DS}^2}{2},$$

$$I_{DS,sat} = \mu\frac{W}{2L}\left[\frac{\varepsilon_0\varepsilon_{\text{SiO}_2}}{t_{\text{SiO}_2}} + \frac{\varepsilon_0\varepsilon_{\text{POM-H}}}{t_{\text{POM-H}}} + \frac{\varepsilon_0\varepsilon_{\text{PEI-EP}}}{t_{\text{PEI-EP}}}\right][V_G - V_t]^2,$$

where $\varepsilon_{\text{SiO}_2}$, $\varepsilon_{\text{POM-H}}$, $\varepsilon_{\text{PEI-EP}}$ are the relative permittivity of the insulators, such as silicone dioxide, POM-H and PEI-EP; t_{SiO_2}, $t_{\text{POM-H}}$, $t_{\text{PEI-EP}}$ is the thickness of the insulators. The current "on–off" ratio is derived by dividing the maximum drain current to the minimum drain current with the same drain voltage. The description of different parameters used in the designed model for evaluating are illustrated in the Table 1 (parameters t_{SiO_2}, $t_{\text{POM-H}}$, $t_{\text{PEI-EP}}$ correspond to t_{ins} in Fig 2 & 3).

Model Parameter Extraction

Electrical characteristics of tri-layer OTFT, such as capacitive insulation, threshold voltage and mobility, are derived using mathematical modeling on Matlab R2020b software with the system configurations of Intel i5-3450S processor at the speed of 2.80 GHz based on 64-bit operating system and 8.0 GB Memory (RAM). In this mathematical model, three dielectric layers, such as SiO_2, POM-H, PEI-EP, are used for improving the electrical conductivity of the transistor. POM-H is the perfect material for components that are meant to replace metal. It provides great stiffness and strength with low friction and high wear resistance. It has a broad operating temperature range (–40 °C to 120 °C) with good stability. Additionally, it mixes well with metals and other polymers that provide great dimensional stability in high precision moulding. Likewise, the third dielectric medium PEI-EP can possess high initial decomposition temperature up to 340 °C. By using these POM-H and PEI-EP layer, the leakage current from the channel will be reduced and this improves the mobility of the free electrons in the channel.

Table 1. Description for the parameters used and derived for the tri-layer OTFT

Parameters	Description	Values
L_{channel}	Channel Length, cm	0.02
W_{channel}	Channel Width, cm	1
T_{OX}	Thickness of the semiconductor, nm	40
V_G	Gate to source Voltage, V	–20 to –80
V_{DS}	Drain to source Voltage, V	–2.5 to –10
ε_0	Permittivity of the vacuum space, F/m	$8.854\cdot10^{-12}$
$\varepsilon_{\text{SiO}_2}$	Relative permittivity of silicone dioxide	3.9
$\varepsilon_{\text{POM-H}}$	Relative permittivity of POM-H	3.8
$\varepsilon_{\text{PEI-EP}}$	Relative permittivity of PEI-EP	3.8
t_{SiO_2}	Thickness of the silicone dioxide insulator, μm	0.3
$t_{\text{POM-H}}$	Thickness of the POM-H insulator, μm	0.8
$t_{\text{PEI-EP}}$	Thickness of the PEI-EP insulator, μm	0.3

I-V characteristics for single-, bi- and tri-layer dielectric medium OTFT

OTFTs are tri-terminal, unipolar, voltage-controlled, high input impedance devices which are used as an integral part for vast variety of electronic circuits. The OTFT devices will be in 'off' state with a minimum current flow between source and drain electrodes when the gate voltage is not applied. If the gate voltage is applied, the electrons or holes can be induced at semiconductor/dielectric interface that increases the source drain current ('on' state). OTFTs are mainly designed using a single dielectric medium for reducing the leakage current and enhancing the current flow at the source-drain channel. Though the single-layer dielectric medium (such as SiO_2) is good in reducing leakage current, the temperature resistance is still a major drawback in the OTFT. Thus, a tri-layer OTFT mathematical model has been derived using organic dielectric medium for enhancing the temperature resistance of the device. Fig. 4 shows the I-V characteristics for single-layer dielectric medium OTFT.

Fig. 4 illustrates the I-V characteristics for three different layer OTFT models. The V_{gs} (V) refers to V_G that represents gate to source voltage which is kept constant for drain current characteristics of MOSFET. In this mathematical model, the gate voltage has been varied for attaining different drain current characteristics of the designed tri-layer OTFT model. I-V characteristic of the OTFT is determined by making the gate voltage (V_G) constant and varying the drain voltage (V_{DS}) to attain the drain current (I_{DS}) of the OTFT. The single-layer OTFT consists of SiO_2 as a dielectric medium, bi-layer consists of SiO_2 and PEI-EP as dielectric medium and tri-layer consists of SiO_2, PEI-EP and POM-H as a dielectric medium. The insulation of the substrate current will be high for the designed tri-layer OTFT due to the three insulation layer, which reduces the leakage current at the source to drain channel.

Table 2 illustrates the attained values of the drain current characteristics for the three different OTFT models. These values of the I_{DS} (mA) are almost similar to the I_{DS} (mA) of single- and bi-layer dielectric medium OTFT model but the resistance of the tri-layer dielectric medium has enhanced the values of the designed tri-layer OTFT than the other OTFT models.

The threshold voltage is abbreviated as V_t which is the least gate-to-source voltage (V_G) required to provide a conducting route between the source and drain terminals. It is a critical scaling factor for maintaining power efficiency. In this evaluation, the threshold voltage of the three different layer OTFT model are demonstrated at Fig. 5.

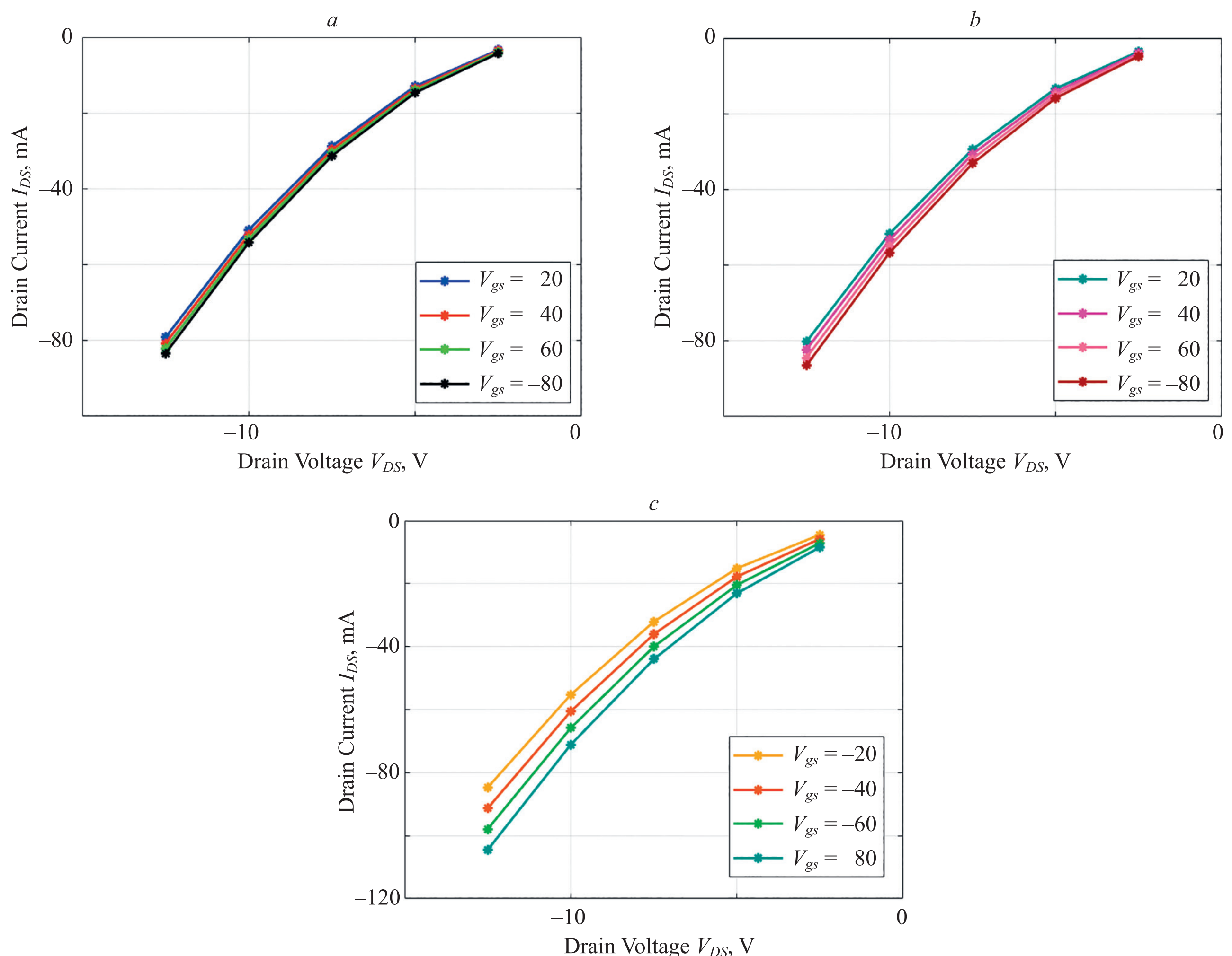

Fig. 4. I-V characteristics for single-layer (*a*), bi-layer (*b*) and tri-layer (*c*) dielectric media

Table 2. I-V characteristics for single-, bi- and tri-layer dielectric medium OTFT models, V

Gate voltage (V_G)	Drain voltage (V_{DS})								
	Single-layer			Bi-layer			Tri-layer		
	–2.5	–5	–7.5	–2.5	–5	–7.5	–2.5	–5	–7.5
–20	–3.33	–12.91	–28.75	–3.54	–13.33	–29.37	–4.44	–15.13	–32.07
–40	–3.64	–13.54	–29.69	–3.96	–14.17	–30.63	–5.76	–17.77	–36.03
–60	–3.91	–14.08	–30.50	–4.37	–15.00	–31.88	–7.08	–20.41	–40.00
–80	–4.18	–14.61	–31.29	–4.79	–15.84	–33.14	–8.40	–23.06	–43.96

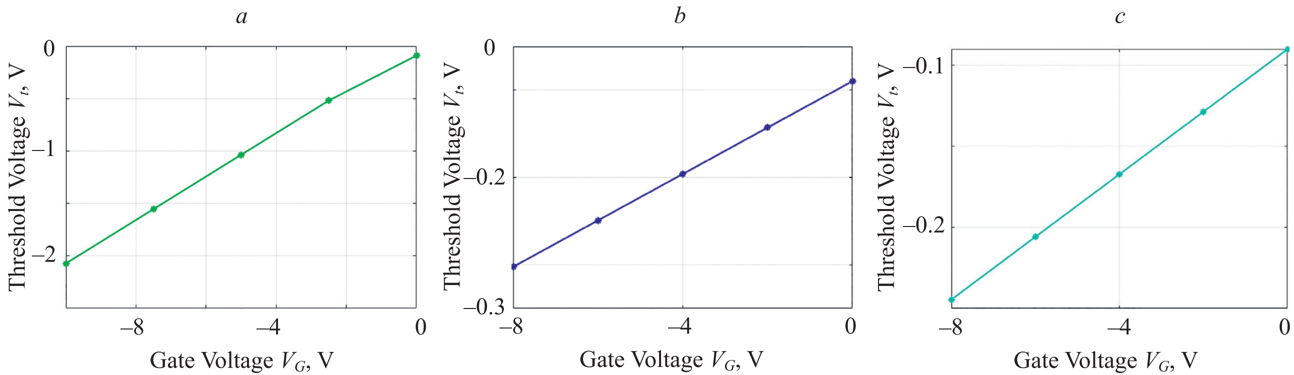

Fig. 5. Threshold voltages for single-layer (*a*), bi-layer (*b*) and tri-layer (*c*) dielectric media of OTFT

Table 3. Threshold voltage vs. gate voltage for different layer structures of dielectric medium OTFT, V

Parameter	Single-layer			Bi-layer			Tri-layer		
Gate voltage (V_G)	–2.5	–5	–7.5	–2.5	–5	–7.5	–2.5	–5	–7.5
Threshold voltage (V_t)	–0.51	–1.03	–1.6	–0.14	–0.19	–0.25	–0.12	–0.16	–0.207

Table 3 illustrates the attained threshold voltage of three different layers OTFT for different gate voltage. Threshold voltage for minimum gate voltage is similar for three different types of OTFT but the maximum gate voltage differs a lot for the different type of OTFTs. The threshold voltage for the tri-layer dielectric medium OTFT model consist of low voltages, lower than single- and bi-layer dielectric medium OTFT model, which results in quick conduction of current among the source and drain channel.

Effective mobility of the single-, bi- and tri-layer OTFT for different pentacene thickness are illustrated at Fig. 6. The OTFT is activated by biasing the gate which begins collecting carriers among the source and drain channels. This attraction is normal to the carrier flow that attracts channel carriers to the semiconductor-oxide interface where they can scatter off the interface. This additional scattering mechanism reduces the mobility of the carriers crossing the channel. Hence, a tri-layer dielectric OTFT has been designed to enhance the mobility of the carrier between the conduction channels.

Table 4 illustrates the effective mobility of three different layer OTFT model for different pentacene thickness. Thus, the evaluation of the effective mobility for three different layer OTFT model shows that the designed

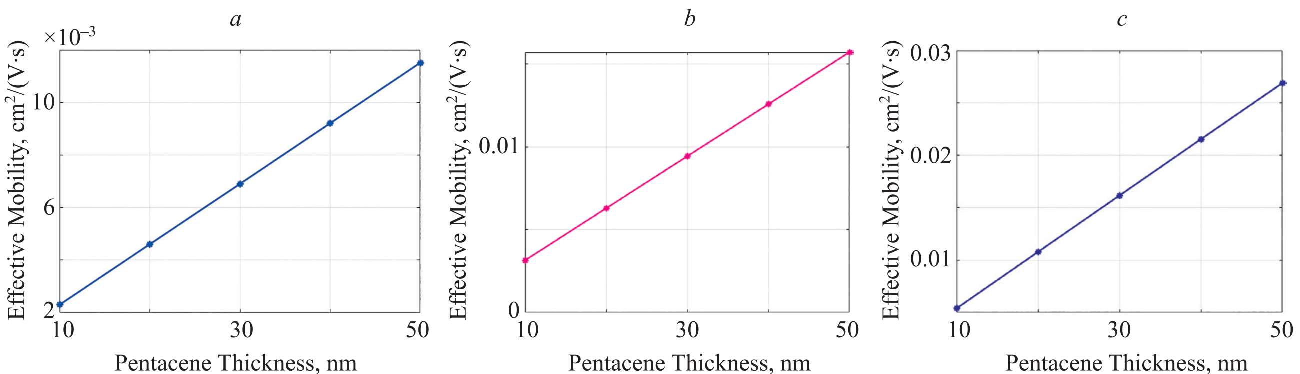

Fig. 6. Effective mobility for single-layer (*a*), bi-layer (*b*) and tri-layer (*c*) OTFT

Table 4. Effective mobility vs. pentacene thickness for different layer structures

Parameter name	Single-layer			Bi-layer			Tri-layer		
Pentacene thickness, nm	10	20	30	10	20	30	10	20	30
Effective mobility, $cm^2/(V \cdot s)$	0.002	0.004	0.006	0.003	0.006	0.009	0.005	0.010	0.016

tri-layer dielectric OTFT based on SiO_2, POM-H and PEI-EP model performs better than the other OTFT model.

Conclusion

Mathematical modelling of tri-layer OTFT has been implemented and compared with the existing OTFT based on different layers of dielectric medium. The proposed tri-layer OTFT model designed in this research work is based on the three dielectric medium, such as SiO_2, POM-H and PE-EP. For evaluating the I-V characteristics of the designed tri-layer OTFT, the pentacene semiconductor is used in this designed model. The evaluated parameters of the designed model are drain current (mA), threshold voltage (V_t) and mobility (μ). The attained I_{DS} (mA) from single-, bi- and tri-layer dielectric medium OTFT model for –20 V gate voltage and –2.5 V drain voltage are –3.33, –3.54 and –4.44. Then, the threshold voltage of the single-, bi- and tri-layer OTFT of 10 V (V_G) are –2.072, –0.3023 and –0.2445. Likewise, the mobility of the three OTFT model for 40 nm pentacene are 0.0092, 0.0125 and 0.0215. Thus, the evaluation of the drain current (mA), mobility (μ) and threshold voltage (V_t) of three different layer dielectric medium OTFT model shows that the performance of the designed tri-layer dielectric medium OTFT model is greater than the other OTFT models. In future, the generated mathematical model will be simulated using computerised software to evaluate the reliability of the designed model performance.

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Conflict of Interest

The authors declared that they have no conflicts of interest to this work. We declare that we do not have any commercial or associative interest that represents a conflict of interest in connection with the work submitted.

Availability of data and material

Not applicable.

Code availability

Not applicable.

Author contributions

The corresponding author claims the major contribution of the paper including formulation, analysis and editing. The co-author provides guidance to verify the analysis result and manuscript editing.

Compliance with ethical standards

This article is a completely original work of its authors; it has not been published before and will not be sent to other publications until the journal’s editorial board decides not to accept it for publication.

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Authors

Deepika Panghal — Research Scholar, Department of ECE, Deenbandhu Chhotu Ram University of Science and Technology, Sonepat, 131039, India, https://orcid.org/0000-0001-6769-0948, deepikapanghal5@gmail.com

Rekha Yadav — D.Sc. Associate Professor, Department of ECE, Deenbandhu Chhotu Ram University of Science and Technology, Sonepat, 131039, India, sc 57208815836, https://orcid.org/0000-0001-9580-9766, Rekhayadav.ece@dcrustm.org

Авторы

Пангал Дипика — магистр, исследователь, Университет науки и технологий Динбандху Чхоту Рам, Сонипат, 131039, Индия, https://orcid.org/0000-0001-6769-0948, deepikapanghal5@gmail.com

Ядав Рекха — доктор наук, доцент, Университет науки и технологий Динбандху Чхоту Рам, Сонипат, 131039, Индия, sc 57208815836, https://orcid.org/0000-0001-9580-9766, Rekhayadav.ece@dcrustm.org

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